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EXAMINER
KEBEDE, BROOK

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 20040406

Application Number: 09/313,424
Filing Date: May 17, 1999
Appellant(s): HUTTNER ET AL.

Markus Nolff
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed January 23, 2004.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellants' statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellants' statement of the issues in the brief is correct.

(7) Grouping of Claims

Appellants' brief includes a statement that claims 16-21 and 23-25 do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

5,468,657	Hsu	11-1995
6,121,117	Sato et al.	9-2000

(10) Grounds of Rejection

A. Claims 16- 21 and 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over unpatentable Hsu (US/5,468,657) in view of Sato et al. (USPAT/6,121,117).

Re claim 16 -19 Hsu teaches a method of fabricating a semiconductor configuration comprising: providing a semiconductor structure (see Fig. 4) having a base layer (44), an insulation layer (59), and a monocrystalline silicon layer (42 or 20); introducing a passivating substance X (34) (i.e., nitrogen ion-implanting) between the insulation layer (59) and the monocrystalline silicon layer (42) having maximum implant concentration of X substance; and heat-treating the semiconductor structure with the passivating substance X, thereby, causing the passivating substrate diffuse into an interface between the insulation layer (59) and the monocrystalline silicon layer (42) (see Fig. 4 and Col. 7, lines 24-45).

However, Hsu does not specifically disclose limitations of providing two silicon semiconductor substrates; oxidizing and forming a respective oxide layer on the two silicon semiconductor substrates; selecting an introducing step from a group consisting of introducing the passivating substance X into at least one of the oxide layers, introducing the passivating substance X before the oxidation step into one of the silicon semiconductor substrates, and introducing the passivating substance X after the oxidation step into one of the silicon semiconductor substrates; joining the two silicon semiconductor substrates by contacting the two

oxide layers; and partially removing one of the silicon semiconductor substrates and forming the monocrystalline silicon layer.

Sato et al. disclose providing two silicon semiconductor substrates; oxidizing and forming a respective oxide layer on the two silicon semiconductor substrates; selecting an introducing step from the group consisting of introducing the passivating substance X into at least one of the oxide layers, introducing the passivating substance X before the oxidation step into one of the silicon semiconductor substrates, and introducing the passivating substance X after the oxidation step into one of the silicon semiconductor substrates; joining the two silicon semiconductor substrates by contacting the two oxide layers; and partially removing one of the silicon semiconductor substrates and forming the monocrystalline silicon layer in order to form SOI (see Figs. 2A-2D).

Sato et al. suggest that "formation of mono-crystalline Si semiconductor layer on an insulator is well known as silicon-on-insulator (SOI) technique. Many investigations have been made thereon since the devices made by the SOI technique have many advantages which are not achievable with a bulk Si substrate for usual Si integrated circuits. The advantages brought about by the SOI technique are as below: 1. Ease of dielectric separation, and practicability of high integration, 2. High resistance against radioactive rays, 3. Low floating capacity, and practicability of high speed operation, 4. Practicability of omission of a welling step, 5. Practicability of prevention of latching-up, 6. Practicability of thin film formation for complete depletion type field effect transistor, and so forth." (see Sato et al. Col. 3, lines 42-59).

Both Hsu and Sato et al. disclosure is directed to formation of SOI substrate and use of the SOI substrate for fabrication of semiconductor devices. Therefore, the teachings of Hsu and Sato et al.is analogous.

One of ordinary skill in the art would have motivated to look to analogous art teaching alternative or useful method of forming of SOI substrate technique as Sato et al. disclosed in order to improve the overall device performance and applicability of the device.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Hsu reference with SOI technique as taught by Sato et al. because the device performance would have been improved.

Re claim 20, as applied to claim 16 above, Hsu and Sato et al. in combination teach all the claimed limitations including the limitation of forming a covering oxide layer (68) on the monocrystalline silicon layer (see Fig. 5).

Re claim 21, as applied to claim 16 above, both Hsu and Sato et al. in combination teach all the claimed limitations including the limitation of patterning the monocrystalline silicon layer by etching away regions thereof down to the underlying insulation layer (see Hsu Figs. 4 and 5).

Re claim 23, as applied to claim 21 above, both Hsu and Sato et al. in combination teach all the claimed limitations including wherein the patterning step performed before the step of introducing the passivating substance X into one of an insulation layer and the monocrystalline silicon layer (see Hsu Figs. 4 and 5).

Re claim 24, as applied to claim 16 above, Hsu and Sato et al. in combination teach all the claimed limitations including the limitation of doping the monocrystalline silicon layer differently region by region by means of ion implantation; and performing the doping step after

the step of introducing the passivating substance X and the heat-treating step (see Col. 8, lines 17-67).

Re claim 25, as applied to claim 21 above, both Hsu and Sato et al. in combination teach all the claimed limitations including wherein the step of introducing the passivating substance X into monocrystalline silicon layer is performed such that an implanted does of the passivating substance X is below an amorphizing dose of silicon (see Hsu Figs. 4 and 5).

Allowable Subject Matter

Claim 22 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

(11) Response to Argument

Appellants' arguments filed on January 23, 2004 have been fully considered but they are not persuasive.

Pertaining to appellants' arguments in Page 13 through Page 16, i.e., "It is clear from Fig. 4 and from the specification of Hsu that in Hsu the nitrogen is placed into the silicon dioxide layer 59 (col. 1, lines 35-36) and is not placed into the silicon layer 42 or monocrystalline silicon In contrast, in the invention of the instant layer 44. application as recited in claim 16, the passivating substance is placed into the monocrystalline silicon layer. Passing the nitrogen trough the monocrystalline silicon layer 42 is not equivalent with placing the nitrogen into the monocrystalline silicon layer 42… There is no disclosure or suggestion in either Hsu or Sato et al. to introduce and place a passivating substance into a monocrystalline silicon layer. Furthermore, neither Hsu nor Sato et al. contain teachings that would underlying realization

suggest the on which the present invention is invention as recited in claim 16 of the based. Therefore, the instant application is believed not to be obvious over Hsu in view of Sato et al ...," the Examiner respectfully submits that such an argument is not commensurate with the scope of the claims, in particularly, as stated above.

The Examiner respectfully submits that the combination of Hsu '657 and Sato et al. '117 teach all the claimed limitations (i.e., the claimed limitations of claims 16-21 and 23-35) as applied in Paragraph 4 of Office action of July 15, 2003. As indicated in the brief (see Pages 14 and 15), appellants admitted that upper layer **42** is monocrystalline silicon, middle layer **59** silicon oxide (dioxide), and lower layer **44** is monocrystalline silicon (see Fig. 4 of Hsu '657 as presented in the brief in Page 14). The only issue is that whether or not the nitrogen ions **34** are implanted in the monocrystalline silicon layer **42**.

Hsu '657, as depicted in Fig. 4, shows that implanting of the first monocrystalline layer **42** with nitrogen ions **34** (i.e., passivating substance X) (see Hsu '657 Col. 7, lines 24-45). Fig. 4 also shows that the depth of the nitrogen implant that reaches the buried oxide layer **59**. Hence, appellants contention "there is no disclosure or suggestion in either Hsu or Sato et al. to introduce and place a passivating substance into a monocrystalline silicon layer" has no merit because there is no way one of ordinary skill in the art would have misconstrued Hsu '657 teachings the way appellants presented. Furthermore, it is well known to one having ordinary skill in the art that monocrystalline silicon has substantially same crystal orientation in the grain structure. Thus, the monocrystalline silicon layer **42** is also implanted by ions **34** during implantation. The depth of ion implantation is a function Gaussian distribution which is dependent on implant energy, ion density, and anneal temperature. In order for appellants to

show that Hsu '657 does not teach implanting the monocrystalline layer **42**, applicants have to provide factual evidence that either the layer **42** is a void layer so that the layer **42** can pass through dopant without being doped or the layer does not exist at all. As a matter of fact, neither is true.

In addition, the claims are given their broadest reasonable interpretation in light of the supporting disclosure. See *In re Morris*, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997). Limitations appearing in the specification but not recited in the claim are not read into the claim. See *In re Prater*, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-551 (CCPA 1969). See also *In re Zletz*, 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989).

Therefore, the *prima facie* case of obviousness has been met and the rejection under 35 U.S.C. § 103 is deemed proper.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Olik Chaudhuri
Supervisory Patent Examiner
Technology Center 2800

BK
April 18, 2004

Appeal conference has been held on March 10, 2004. The conferees are listed herein below.

1. Olik Chaudhuri, Chair Person and SPE Art Unit 2823. OC
2. Wael M. Fahmy, SPE Art Unit 2814. W.F
3. Brook Kebede, Examiner Art Unit 2823. BK

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